THAT WHICH IS CLAIMED IS:

1. A digital delay line, comprising:

a cascaded string of delay elements that has a plurality of injection ports and is responsive to an injection control signal that designates which of the plurality of injection ports is enabled to accept an input signal to be delayed.

2. The delay line of Claim 1, wherein the plurality of injection ports are electrically coupled together.

3. The delay line of Claim 2, wherein each of the plurality of injection ports comprises a respective pair of differential injection terminals.

4. The delay line of Claim 3, wherein each of a plurality of true injection terminals associated with the plurality of injection ports are electrically connected together; and wherein each of a plurality of complementary injection terminals associated with the plurality of injection ports are electrically coupled together.

5. The delay line of Claim 4, wherein the injection control signal is a multi-bit wide signal; and wherein each of a plurality of delay elements in said cascaded string of delay elements has a pair of differential inputs and a pair of differential outputs.

6. The delay line of Claim 5, wherein each of the plurality of delay elements in said cascaded string of delay elements is responsive to first and second bias signals that are floated at first and second voltage levels, respectively, when said cascaded string of delay elements is active.

7. The delay line of Claim 6, further comprising first and second bias signal generators that are configured to generate the first and second bias signals, respectively, in response to a strobe signal.

8. The delay line of Claim 1, wherein each of a plurality of delay elements in said cascaded string of delay elements has a pair of differential inputs and a pair of differential outputs.

9. The delay line of Claim 8, wherein each of the plurality of delay elements in said cascaded string of delay elements is responsive to a first floating bias signal that tracks variations in a power supply voltage provided to said cascaded string of delay elements.

10. The delay line of Claim 1, wherein each of a plurality of delay elements in said cascaded string of delay elements is responsive to first and second floating bias signals that are provided on first and second bias signal lines, respectively.

11. The delay line of Claim 10, further comprising:

a first bias signal generator that is configured to intermittently pump the first bias signal line with displacement current; and

a second bias signal generator that is configured to intermittently pump the second bias signal line with displacement current.

12. The delay line of Claim 11, wherein said first and second bias signal generators are configured to provide high impedance outputs to said first and second bias signal lines, respectively, when said cascaded string of delay elements is active.

13. The delay line of Claim 12, wherein said first bias signal generator comprises:

a first capacitor having a first electrode electrically connected to a first intermediate bias node;

a first switch having first and second current carrying terminals electrically connected to the first intermediate bias node and the first bias signal line, respectively; and

a second switch having first and second current carrying terminals electrically connected to the first intermediate bias node and a reference line, respectively.

14. The delay line of Claim 13, wherein a second electrode of said first capacitor is electrically connected to a power supply line.

15. The delay line of Claim 14, wherein said second bias signal generator comprises:

a second capacitor having a first electrode electrically connected to a second intermediate bias node;

a third switch having first and second current carrying terminals electrically connected to the second intermediate bias node and the second bias signal line, respectively; and

a fourth switch having a first current carrying terminal electrically coupled to the second intermediate bias node.

16. The delay line of Claim 15, wherein a second electrode of said second capacitor is electrically connected to the reference line.

17. The delay line of Claim 16, wherein said second bias signal generator comprises a voltage divider; and wherein said fourth switch comprises a second current carrying terminal electrically connected to an output of said voltage divider.

18. The delay line of Claim 17, wherein said voltage divider comprises:

a normally-on PMOS pull-up transistor; and

an NMOS pull-down transistor having gate and drain terminals that are commonly connected to a drain terminal of said normally-on PMOS pull-up transistor at the output of said voltage divider.

19. The delay line of Claim 13, wherein said first and second switches comprise first and second MOS transistors, respectively; and wherein said first bias signal generator comprises a first bias control circuit that is electrically coupled to gate electrodes of the first and second MOS transistors.

20. The delay line of Claim 19, wherein the first bias control circuit is responsive to a strobe signal and a reset signal.

21. The delay line of Claim 20, wherein the first bias control circuit is configured to turn on the first and second switches simultaneously when the reset signal is active.

22. The delay line of Claim 15, wherein said first, second, third and fourth switches comprise first, second, third and fourth MOS transistors, respectively; wherein said first bias signal generator comprises a first bias control circuit that is electrically coupled to gate electrodes of the first and second MOS transistors; and wherein said second bias signal generator comprises a second bias control circuit that is electrically coupled to gate electrodes of the third and fourth MOS transistors.

23. The delay line of Claim 22, wherein the first and second bias control circuits are configured to turn on the first, second, third and fourth switches simultaneously in response to an active reset signal.

24. The delay line of Claim 1, wherein the injection control signal is a multi-bit wide signal; and wherein each of a plurality of delay elements in said cascaded string of delay elements comprises an injection control terminal that receives a respective bit of the injection control signal.

25. The delay line of Claim 24, further comprising a decoder having a plurality of outputs that are electrically coupled to the injection control terminals of the plurality of delay elements.

26. An integrated circuit delay element, comprising:

a differential amplifier having a pair of differential inputs and a pair of differential outputs;

a first load transistor having a first current carrying terminal electrically coupled to a true one of the pair of differential outputs;

a second load transistor having a first current carrying terminal electrically coupled to a complementary one of the pair of differential outputs;

a first bias signal line electrically coupled to gate electrodes of said first and second load transistors; and

a first bias signal generator that is configured to float said first bias signal line at a first bias voltage when said differential amplifier is active.

27. The delay element of Claim 26, wherein second current carrying terminals of said first and second load transistors are electrically coupled to a power supply line.

28. The delay element of Claim 27, wherein said first bias signal generator is configured to intermittently pump said first bias signal line with displacement current during when said differential amplifier is inactive.

29. The delay element of Claim 28, wherein said first bias signal generator comprises:

a pull-up capacitor having a first electrode electrically coupled to the power supply line; and

a first switch having a first current carrying terminal electrically connected to a second electrode of said pull-up capacitor and a second current carrying terminal electrically connected to said first bias signal line.

30. The delay element of Claim 29, wherein a capacitance of said first bias signal line is greater than about 100 times a capacitance of said pull-up capacitor.

31. The delay element of Claim 29, wherein said first bias signal generator further comprises a second switch having a first current carrying terminal electrically connected to the second electrode of said pull-up capacitor and a second current carrying terminal electrically connected to a reference line.

32. The delay element of Claim 26, wherein said first bias signal generator is configured to pump said first bias signal line with positive displacement current during at least a first interval when said differential amplifier is inactive and is further configured to pump said first bias signal line with negative displacement current during at least a second interval when said differential amplifier is inactive.

33. The delay element of Claim 26, wherein said differential amplifier comprises:

a first pair of input transistors having first current carrying terminals that are electrically connected together; and

a pull-down current source electrically coupled to the first current carrying terminals of said first pair of input transistors.

34. The delay element of Claim 33, further comprising:

a second bias signal line electrically connected to a control input of said pull-down current source; and

a second bias signal generator that is configured to float said second bias signal line at a second bias voltage when said differential amplifier is active.

35. The delay element of Claim 34, wherein said second bias signal generator is configured to intermittently pump said second bias signal line with displacement current when said differential amplifier is inactive.

36. The delay element of Claim 34, wherein said second bias signal generator is configured to pump said second bias signal line with positive or negative displacement current when said differential amplifier is inactive.

37. The delay element of Claim 35, wherein a capacitance of said second bias signal line is greater than about 100 times a capacitance of said pull-down capacitor; and wherein said second bias signal generator comprises:

a pull-down capacitor having a first electrode electrically coupled to a ground reference line; and

a first switch having a first current carrying terminal electrically connected to a second electrode of said pull-down capacitor and a second current carrying terminal electrically connected to said second bias signal line.

38. The delay element of Claim 37, wherein said second bias signal generator further comprises:

a second switch having a first current carrying terminal electrically connected to the second electrode of said pull-down capacitor; and

a voltage divider that is electrically coupled between a power supply line and the ground reference line and has an output that is electrically connected to a second current carrying terminal of said second switch.

39. The delay element of Claim 33, wherein said pull-down current source comprises a totem pole arrangement of first and second NMOS pull-down transistors that extend between the first current carrying terminals of said first pair of input transistors and a reference line.

40. The delay element of Claim 39, wherein a gate electrode of the first NMOS pull-down transistor is responsive to an injection control signal; and wherein a gate electrode of the second NMOS pull-down transistor is electrically connected to a second bias signal line.

41. The delay element of Claim 40, further comprising a second bias signal generator that is configured to float the second bias signal line when said differential amplifier is active and is further configured to intermittently pump the second bias signal line with displacement current when said differential amplifier is inactive.

42. An integrated circuit delay element, comprising:

a differential amplifier having a pair of differential inputs and a pair of differential outputs, said differential amplifier comprising a first pair of NMOS input transistors having commonly connected first current carrying terminals and a pull-down current source electrically coupled to the first current carrying terminals of said first pair of input transistors;

a first PMOS load transistor having a first current carrying terminal electrically coupled to a true one of the pair of differential outputs and a second current carrying terminal electrically coupled to a power supply line;

a second PMOS load transistor having a first current carrying terminal electrically coupled to a complementary one of the pair of differential outputs and a second current carrying terminal electrically coupled to the power supply line;

a first bias signal line electrically coupled to gate electrodes of said first and second PMOS load transistors;

a first bias signal generator that is configured to float said first bias signal line at a first bias voltage when said differential amplifier is active and is further configured to pump said first bias signal line with positive or negative displacement current when said differential amplifier is inactive;

a second bias signal line electrically connected to a control input of the pull-down current source; and

a second bias signal generator that is configured to float said second bias signal line at a second bias voltage when said differential amplifier is active and is further configured to pump said second bias signal line with positive or negative displacement current when said differential amplifier is inactive.

43. A ring oscillator, comprising:

first and second bias signal lines;

a plurality of differential amplifier delay elements having respective load devices that are electrically coupled to said first bias signal line and respective current sources that are electrically coupled to said second bias signal line;

a first bias signal generator that is configured to pump said first bias signal line with displacement current when enabled; and

a second bias signal generator that is configured to pump said second bias signal line with displacement current when enabled.

44. The ring oscillator of Claim 43, wherein said first bias signal generator is further configured to float said first bias signal line when disabled.

45. The ring oscillator of Claim 44, wherein the load devices are PMOS pull-up transistors having gate electrodes electrically coupled to said first bias signal line.

46. The ring oscillator of Claim 43, wherein each pair of differential outputs of said plurality of differential amplifier delay elements has a respective dual-terminal injection port coupled thereto.

47. The ring oscillator of Claim 46, wherein each of the plurality of injection ports comprises a respective pair of differential injection terminals.

48. The ring oscillator of Claim 47, wherein each of said plurality of differential amplifier delay elements comprises an injection control terminal that receives a respective bit of a multi-bit wide injection control signal.

49. An integrated circuit delay device, comprising:

a digital delay line that is configured to provide a percent-of-clock period delay to a timing signal received at an input thereof, in response to a control signal; and

a delay line control circuit that is electrically coupled to said digital delay line, said delay line control circuit comprising:

a ring oscillator;

a counter that is configured to record a number of oscillations generated by the ring oscillator over a first time interval; and

decoding logic that is configured to generate the control signal in response to the number of oscillations recorded by said counter.

50. The delay device of Claim 49, wherein the oscillations generated by the ring oscillator have a period that is shorter than the percent-of-clock period delay provided by said digital delay line.

51. The delay device of Claim 50, wherein a duration of the first time interval is at least ten times greater than the period of the oscillations generated by the ring oscillator.

52. The delay device of Claim 51, wherein the duration of the first time interval is at least ten times greater than the percent-of-clock period delay provided by said digital delay line.

53. The delay device of Claim 49, wherein said delay line control circuit is responsive to a system clock signal; and wherein the ring oscillator is responsive to an enable clock signal having a period that is N times greater than a period of the system clock signal, where N is a positive integer.

54. The delay device of Claim 49, wherein said delay line control circuit comprises a divide-by-N clock generator having an input that is responsive to a system clock signal and a first output electrically coupled to an enable input of the ring oscillator, where N is a positive integer.

55. The delay device of Claim 54, wherein said delay line control circuit comprises a first pulse generator that is configured to decode a first plurality of outputs of the divide-by-N clock generator into a first pulse signal that is provided to a reset input of the counter.

56. The delay device of Claim 55, wherein the decoding logic comprises a first multi-bit wide latch having data inputs electrically coupled to outputs of the counter.

57. The delay device of Claim 56, wherein said delay line control circuit comprises a second pulse generator that is configured to decode a second plurality of outputs of the divide-by-N clock generator into a second pulse signal that is provided to a store input of the first multi-bit wide latch.

58. The delay device of Claim 56, wherein the decoding logic comprises a second multi-bit wide latch having data inputs electrically coupled to data outputs of the first multi-bit wide latch.

59. The delay device of Claim 58, wherein the decoding logic comprises a decoder having a plurality of inputs that are electrically coupled to data outputs of the second multi-bit wide latch.

60. An integrated circuit delay device, comprising:

a digital delay line that is configured to provide a percent-of-clock period delay to a timing signal received at an input thereof, in response to a control signal having a value that specifies a length of the delay; and

a delay line control circuit that is configured to generate the control signal by counting multiple cycles of a high frequency oscillator signal having a period less than the clock period, over a time interval having a duration greater than the clock period.

61. The delay device of Claim 60, wherein said digital delay line comprises a cascaded string of delay elements having a plurality of injection ports electrically coupled together.

62. The delay device of Claim 61, wherein the control signal comprises a multi-bit injection control signal that designates which one of the plurality of injection ports is enabled to accept the timing signal.

63. The delay device of Claim 62, wherein each of the plurality of injection ports comprises a respective pair of differential injection terminals.

64. The delay device of Claim 63, wherein each of a plurality of true injection terminals associated with the plurality of injection ports are electrically connected together; and wherein each of a plurality of complementary injection terminals associated with the plurality of injection ports are electrically coupled together.

65. The delay device of Claim 64, wherein each of a plurality of delay elements in said cascaded string of delay elements has a pair of differential inputs and a pair of differential outputs.

66. The delay device of Claim 65, wherein each of the plurality of delay elements in said cascaded string of delay elements is responsive to first and second floating bias signals.

67. The delay device of Claim 66, wherein said delay line control circuit comprises first and second bias signal generators that are configured to generate the first and second floating bias signals, respectively, in response to a strobe signal.

68. The delay device of Claim 61, wherein each of a plurality of delay elements in the cascaded string of delay elements is responsive to first and second bias floating signals that are provided on first and second bias signal lines, respectively.

69. The delay device of Claim 68, further comprising:

a first bias signal generator that is configured to intermittently pump the first bias signal line with displacement current; and

a second bias signal generator that is configured to intermittently pump the second bias signal line with displacement current.

70. The delay device of Claim 69, wherein said first and second bias signal generators are configured to provide high impedance outputs to said first and second bias signal lines, respectively, when the cascaded string of delay elements is active.

71. The delay device of Claim 70, wherein said first bias signal generator comprises:

a first capacitor having a first electrode electrically connected to a first intermediate bias node;

a first switch having first and second current carrying terminals electrically connected to the first intermediate bias node and the first bias signal line, respectively; and

a second switch having first and second current carrying terminals electrically connected to the first intermediate bias node and a reference line, respectively.

72. The delay device of Claim 71, wherein a second electrode of said first capacitor is electrically connected to a power supply line.

73. The delay device of Claim 72, wherein said second bias signal generator comprises:

a second capacitor having a first electrode electrically connected to a second intermediate bias node;

a third switch having first and second current carrying terminals electrically connected to the second intermediate bias node and the second bias signal line, respectively; and

a fourth switch having a first current carrying terminal electrically coupled to the second intermediate bias node.

74. The delay device of Claim 73, wherein a second electrode of said second capacitor is electrically connected to the reference line.

75. The delay device of Claim 74, wherein said second bias signal generator comprises a voltage divider; and wherein said fourth switch comprises a second current carrying terminal electrically connected to an output of said voltage divider.

76. The delay device of Claim 75, wherein said voltage divider comprises:

a normally-on PMOS pull-up transistor; and

an NMOS pull-down transistor having gate and drain terminals that are commonly connected to a drain terminal of said PMOS pull-up transistor at the output of said voltage divider.

77. An integrated circuit delay device, comprising:

a digital delay line that is configured to provide a percent-of-clock period delay to a timing signal accepted at an enabled one of a plurality of injection ports thereof, in response to an injection control signal having a value that sets a length of the delay by specifying a location of the enabled one of the plurality of injection ports; and

a delay line control circuit that is configured to generate the injection control signal by counting multiple cycles of a high frequency ring oscillator signal having a period less than the clock period, over a time interval having a duration greater than the clock period.

78. The delay device of Claim 77, wherein said digital delay line comprises a cascaded string of delay elements that are each connected to a respective one of the plurality of injection ports; and wherein the plurality of injection ports are electrically coupled together.

79. The delay device of Claim 78, wherein the injection control signal comprises a multi-bit injection control signal that designates which one of the plurality of injection ports is enabled to accept the timing signal and disables the delay element associated with the enabled injection port.

80. The delay device of Claim 78, wherein each of the plurality of injection ports comprises a respective pair of differential injection terminals.

81. The delay device of Claim 80, wherein each of a plurality of true injection terminals associated with the plurality of injection ports are electrically connected together; and wherein each of a plurality of complementary injection terminals associated with the plurality of injection ports are electrically coupled together.

82. The delay device of Claim 81, wherein each of a plurality of delay elements in the cascaded string of delay elements has a pair of differential inputs and a pair of differential outputs.

83. The delay device of Claim 77, wherein said digital delay line comprises a cascaded string of differential amplifier delay elements.

84. The delay device of Claim 83, wherein each of a plurality of delay elements in the cascaded string comprises a pair of PMOS load transistors having gate electrodes electrically coupled to a first bias signal line; and wherein said delay line control circuit comprises a first bias signal generator that is configured to float the first bias signal line at a first bias voltage when said digital delay line is active.

85. The delay device of Claim 84, wherein the first bias signal generator is configured to intermittently pump the first bias signal line with displacement current when said digital delay line is inactive.

86. The delay device of Claim 85, wherein said delay line control circuit comprises a ring oscillator having a plurality of differential amplifier delay elements therein that each comprise a pair of PMOS load transistors having gate electrodes electrically coupled to the first bias signal line.

87. The delay device of Claim 86, wherein the first bias signal generator comprises:

a pull-up capacitor having a first electrode electrically coupled to a power supply line; and

a first switch having a first current carrying terminal electrically connected to a second electrode of said pull-up capacitor and a second current carrying terminal electrically connected to the first bias signal line.

88. The delay device of Claim 87, wherein a capacitance of the first bias signal line is greater than about 100 times a capacitance of the pull-up capacitor.

89. The delay device of Claim 86, where the plurality of differential amplifier delay elements in the ring oscillator are equivalent to the plurality of delay elements in the cascaded string.

90. The delay device of Claim 77, wherein said delay line control circuit comprises:

a ring oscillator; and

a divide-by-N clock generator having an input that is responsive to a system clock signal and a first output electrically coupled to an enable input of the ring oscillator, where N is a positive integer.

91. The delay device of Claim 90, wherein said delay line control circuit comprises:

a counter that is electrically coupled to an output of said ring oscillator; and

a first pulse generator that is configured to decode a first plurality of outputs of the divide-by-N clock generator into a first pulse signal that is provided to a reset input of the counter.

92. The delay device of Claim 91, wherein said delay line control circuit comprises a first multi-bit wide latch having data inputs electrically coupled to outputs of the counter.

93. The delay device of Claim 92, wherein said delay line control circuit comprises a second pulse generator that is configured to decode a second plurality of outputs of the divide-by-N clock generator into a second pulse signal that is provided to a store input of the first multi-bit wide latch.

94. The delay device of Claim 92, wherein said delay line control circuit further comprises a second multi-bit wide latch having data inputs electrically coupled to data outputs of the first multi-bit wide latch.

95. The delay device of Claim 94, wherein said delay line control circuit comprises a decoder having a plurality of inputs that are electrically coupled to data outputs of the second multi-bit wide latch.

96. An integrated circuit delay device, comprising:

a digital delay line that is configured to provide a percent-of-clock period delay to a timing signal accepted at an enabled injection port thereof, in response to a control signal having a value that specifies a number of active delay elements between the enabled injection port and an output of said digital delay line; and

a delay line control circuit that is configured to generate the control signal by counting multiple cycles of an oscillator signal having a period less than the clock period, over a time interval having a duration greater than the clock period.

97. An integrated circuit delay device, comprising:

a digital delay line that is configured to provide a timing delay to a differential timing signal received at an input thereof, in response to a control signal having a value that specifies a number of active delay elements in said digital delay line; and

a delay line control circuit that is configured to generate the control signal by counting multiple consecutive cycles of a ring oscillator signal having a period less than a length of the timing delay, over a time interval having a duration greater than the length of the timing delay.

98. An integrated circuit delay device, comprising:

a digital delay line that is configured to provide a percent-of-clock period delay to a timing signal accepted at an injection port thereof, in response to a multi-bit control signal having a value that specifies a number of active differential amplifier delay elements in said digital delay line; and

a delay line control circuit that is configured to generate the multi-bit control signal by counting multiple cycles of a ring oscillator signal having a period less than the clock period, over a time interval having a duration greater than the clock period.

99. The delay device of Claim 98, wherein the ring oscillator signal has a period less than about twenty percent of the clock period; and wherein the time interval has a duration greater than about five times the clock period.

100. A ring oscillator, comprising:

a first bias signal line;

a ring of differential amplifier delay elements having respective load devices that are electrically coupled to said first bias signal line; and

a first bias signal generator that is configured to float said first bias signal line at a first bias voltage when said ring of differential amplifier delay elements is active and is further configured to intermittently pump said first bias signal line with displacement current when said ring of differential amplifier delay elements is inactive.

101. A digital delay line, comprising:

a first bias signal line;

a cascaded string of differential amplifier delay elements having respective load devices that are electrically coupled to said first bias signal line; and

a first bias signal generator that is configured to float said first bias signal line at a first bias voltage when said cascaded string of differential amplifier delay elements is active and is further configured to intermittently pump said first bias signal line with displacement current when said cascaded string of differential amplifier delay elements is inactive.

102. A digital delay line, comprising:

at least one differential amplifier delay element having an injection port that is responsive to an injection control signal and a pair of differential outputs that are electrically coupled to the injection port.

103. The digital delay line of Claim 102, wherein said at least one differential amplifier delay element comprises a current source that is responsive to the injection control signal.

104. An integrated circuit delay line, comprising:

a differential amplifier delay element having a pair of differential inputs and a pair of differential outputs, said differential amplifier comprising a first pair of NMOS input transistors having commonly connected first current carrying terminals and a pull-down current source electrically coupled to the first current carrying terminals of said first pair of input transistors;

a first PMOS load transistor having a first current carrying terminal electrically coupled to a true one of the pair of differential outputs and a second current carrying terminal electrically coupled to a power supply line;

a second PMOS load transistor having a first current carrying terminal electrically coupled to a complementary one of the pair of differential outputs and a second current carrying terminal electrically coupled to the power supply line; and

an injection port that is electrically coupled to the pair of differential outputs.

105. The delay line of Claim 104, wherein said injection port comprises a true injection terminal switch that is electrically coupled to the true one of the pair of differential outputs and a complementary injection terminal switch that is electrically coupled to the complementary one of the pair of differential outputs.

106. The delay line of Claim 105, wherein the true injection terminal switch and the complementary injection terminal switch have commonly connected control terminals that are responsive to an injection control signal.

107. The delay line of Claim 106, wherein the pull-down current source is responsive to the injection control signal and is configured to be inactive when the injection control signal is active at a level that opens the injection port by turning on the true and complementary injection terminal switches.

108. The delay line of Claim 107, wherein the true and complementary injection terminal switches are MOS transistors.

109. The delay line of Claim 108, wherein the true and complementary injection terminal switches are electrically coupled to a pair of differential timing signal lines.

110. The delay line of Claim 107, further comprising:

a first bias signal line electrically coupled to gate electrodes of said first and second PMOS load transistors;

a first bias signal generator that is configured to float said first bias signal line at a first bias voltage when said differential amplifier is active and is further configured to pump said first bias signal line with positive or negative displacement current when said differential amplifier is inactive;

a second bias signal line electrically connected to a control input of the pull-down current source; and

a second bias signal generator that is configured to float said second bias signal line at a second bias voltage when said differential amplifier is active and is further configured to pump said second bias signal line with positive or negative displacement current when said differential amplifier is inactive.

111. The delay line of Claim 104, further comprising:

a first bias signal line electrically coupled to gate electrodes of said first and second PMOS load transistors;

a first bias signal generator that is configured to float said first bias signal line at a first bias potential when said differential amplifier is active and is further configured to pump said first bias signal line with positive or negative displacement current when said differential amplifier is inactive;

a second bias signal line electrically connected to a control input of the pull-down current source; and

a second bias signal generator that is configured to float said second bias signal line at a second bias potential when said differential amplifier is active and is further configured to pump said second bias signal line with positive or negative displacement current when said differential amplifier is inactive.

112. An integrated circuit system, comprising:

a first integrated circuit chip that is configured to generate data and strobe signals at outputs thereof; and

a second integrated circuit chip that receives the data and strobe signals and latches a buffered version of the data signal in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed timing signal, said second integrated circuit chip having a delay device therein that comprises a digital delay line having a plurality of injection ports, said digital delay line configured to generate the delayed timing signal by adding at least a percent-of-clock period delay to a timing signal that is derived from the strobe signal and accepted at an enabled one of the plurality of injection ports of the digital delay line, and further configured to be responsive to an injection control signal having a value that sets a length of the delay by specifying a location of the enabled one of the plurality of injection ports.

113. The integrated circuit system of Claim 112, wherein said delay device is responsive to a system clock signal having a period that sets the length of the period from which the percent-of-clock period delay is measured; and wherein said first integrated circuit chip is responsive to a buffered version of the system clock signal.

114. The integrated circuit system of Claim 113, wherein said first integrated circuit chip comprises a delay locked loop that receives the buffered version of the system clock signal.

115. The integrated circuit system of Claim 112, wherein said first integrated circuit chip comprises a dual data rate (DDR) memory device.

116. The integrated circuit system of Claim 115, wherein the dual data rate (DDR) memory device is a DDR FIFO, said DDR FIFO comprising a plurality of memory devices that are configured to support any combination of dual data rate (DDR) or single data rate (SDR) write modes that operate in-sync with a write clock signal and DDR or SDR read modes that operate in-sync with a read clock signal.

117. An integrated circuit system, comprising:

a dual data rate (DDR) memory chip that is configured to generate a DDR data signal and a DQS strobe signal at respective outputs thereof; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and captures a buffered version of the DDR data signal at a bandwidth of greater than about 200 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller having a digital delay line therein that is configured to generate the delayed DQS strobe signal by adding at least a percent-of-clock period delay to a buffered version of the received DQS strobe signal, and is further configured to be responsive to a multi-bit injection control signal having a value that sets a length of the delay.

118. The integrated circuit system of Claim 117, wherein the buffered version of the received DQS strobe signal is accepted at an enabled one of a plurality of injection ports of the digital delay line; and wherein the multi-bit injection control signal sets the length of the delay by specifying a location of the enabled one of the plurality of injection ports.

119. The integrated circuit system of Claim 117, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to intermittently pump the first bias signal line with displacement current.

120. The integrated circuit system of Claim 117, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to float the first bias signal line at a first voltage level when the string of delay elements are active.

121. The integrated circuit system of Claim 120, the first bias signal generator is further configured to intermittently pump the first bias signal line with displacement current when the string of delay elements is inactive.

122. An integrated circuit system, comprising:

a dual data rate (DDR) memory chip that is configured to generate a DDR data signal and a DQS strobe signal having a frequency of about 133 MHz at respective outputs thereof; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and is configured to capture a buffered version of the DDR data signal at a bandwidth of about 266 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller having a digital delay line therein that is configured to generate the delayed DQS strobe signal by adding about a twenty percent-of-clock period delay to a buffered version of the DQS strobe signal.

123. The integrated circuit system of Claim 122, wherein a data valid window associated with the buffered version of the DDR data signal at the time of capture is in a range between about 1.6 ns and about 1.65 ns.

124. The integrated circuit system of Claim 123, wherein a delay error margin associated with the digital delay line is no greater than about ±0.2 ns over rated ranges of temperature and power supply voltage variations.

125. The integrated circuit system of Claim 122, wherein a delay error margin associated with the digital delay line is no greater than about ±0.2 ns over rated ranges of temperature and power supply voltage variations.

126. The integrated circuit system of Claim 122, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to intermittently pump the first bias signal line with displacement current.

127. The integrated circuit system of Claim 122, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to float the first bias signal line at a first voltage level when the string of delay elements are active.

128. The integrated circuit system of Claim 127, the first bias signal generator is further configured to intermittently pump the first bias signal line with displacement current when the string of delay elements is inactive.

129. The integrated circuit system of Claim 122, wherein a data valid window associated with the buffered version of the DDR data signal at the time of capture is in a range between about 1.55 ns and about 1.70 ns.

130. An integrated circuit system, comprising:

a dual data rate (DDR) memory chip that is configured to generate a DDR data signal and a DQS strobe signal at respective outputs thereof; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and captures a buffered version of the DDR data signal at a bandwidth of greater than about 200 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller comprising:

a digital delay line having a plurality of delay elements therein that are configured to generate the delayed DQS strobe signal by adding at least a percent-of-clock period delay to a buffered version of the received DQS strobe signal;

a first bias signal line that is electrically coupled to bias nodes associated with the plurality of delay elements; and

a bias signal generator that is configured to float the first bias signal line at a first voltage level when the plurality of delay elements are active.

131. The integrated circuit system of Claim 130, wherein said bias signal generator is further configured to periodically pump said first bias signal line with displacement current when the plurality of delay elements are inactive.

132. The integrated circuit system of Claim 130, wherein said DDR memory controller comprises a delay tree therein that is responsive to a system clock signal.

133. An integrated circuit system, comprising:

a dual data rate (DDR) memory chip that is configured to generate a DDR data signal and a DQS strobe signal at respective outputs thereof; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and captures a buffered version of the DDR data signal at a bandwidth of greater than about 200 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller comprising:

a digital delay line having a plurality of delay elements therein that are configured to generate the delayed DQS strobe signal by adding at least a percent-of-clock period delay to a buffered version of the received DQS strobe signal; and

a bias signal generator that is configured to periodically pump a respective bias node associated with each of the plurality of delay elements with displacement current when the plurality of delay elements are inactive.

134. An integrated circuit system, comprising:

a dual data rate (DDR) FIFO that is configured to generate a DDR data signal and a DQS strobe signal at respective outputs thereof and comprises a plurality of memory devices that are configured to support any combination of DDR or single data rate (SDR) write modes that operate in-sync with a write clock signal and DDR or SDR read modes that operate in-sync with a read clock signal; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and captures a buffered version of the DDR data signal at a bandwidth of greater than about 200 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller comprising a digital delay line having a plurality of delay elements therein that are configured to generate the delayed DQS strobe signal by adding at least a percent-of-clock period delay to a buffered version of the received DQS strobe signal.